Jameco Part number 148734

Vitrax Plus^{tm} Controller

A/D CONVERTER MODULE

Document # 950204-AD

ANALOG to DIGITAL CONVERTER

INSTALLATION PROCEDURE
HARDWARE ARRANGEMENT
SOFTWARE SUPPORT

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ANALOG/DIGITAL MODULE

OVERVIEW: The A/D Converter Module provides 8 channels for the Vitrax Plus Controller to convert analog signals to 10-bit digital data. The module contains 5 components that install on the Controller board including U23, a CMOS integrated device that uses a successive approximation method to perform the digital conversion. A 20-pin edge connector at J12 provides an input port. The reference voltage is adjustable via trimpot POT2. To ensure stability and accuracy, a grounded guard ring with ground plane is designed into the P/C board.

ASSEMBLY: Refer to the Component Arrangement Diagram on the last page. To install the A/D module, follow the assembly sequence provided below. It is good practice to socket LSI devices in case of replacement or troubleshooting. The A/D converter requires a 28-pin socket with a width of 0.4" and 0.1" lead spacing. Sockets with these dimensions are unavailable commercially, so 14-pin IC strips are provided. When installing the IC strips, mount them at right angles to the board. First solder one pin on each strip; use a pin near the center. Check that the pin-to-pin spacing from one strip to the other is 0.4". Maintain this dimension while soldering the remaining 26 pins. Solder trimpot POT2 so that the adjustment screw faces the edge of the board - the edge with the DB9 connectors.

Insert the A/D Converter, U23, into the IC strips. Pin 1 must be oriented at the lower left corner (near POT2). Note that the screened legend "U23" at pin 1.

ASSEMBLY SEQUENCE

COMPONENT	DESCRIPTION	COMMENTS
Z23	IC strips: 14-pin (2)	Row-to-row width = 0.4"
POT2	5K (10K) Trimpot	Adj screw toward board edge
J12	2x10 Connector	Edge connector
U23	7004 IC Converter	CMOS - handle carefully

A stable well regulated voltage supply (industrial quality) is required for reliable and accurate operation.

ARCHITECTURE: The A/D Converter occupies two read/write addresses in I/O space: 144 and 145 (decimal). The chart below lists the functions that exist at each address together with the associated data bits. Explanation of the functions follow the table:

CONVERTER REGISTERS			
ADR	**R/W**	**FUNCTION**	**DATA BITS**
145	Write	Data Format	DB2 (0=bin, 1=twos comp)
145	Write	Freq divide ratio	DB1 (msb), DBO: 1/1 to 1/8
144	Write	Select Data channel 0-7	DB2 (msb), DBO, (lsb)
145	Read	Data bits 9-2	DB7 = Data bit 9: DB0 = bit 2
144	Read	Data bits 1,0	DB7 = Data bit 1: DB6 = bit 0

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The format of the digital data can be selected for either binary or twos complement output. Binary data is provided by initializing U23 with a "0" in DB2 at I/O address 145; a logical "1" generates two complement format. (DB1 and DB0 at this address specify the frequency ratio).

The internal frequency of U23 can be matched to the input clock frequency by selecting an appropriate divide ratio: Ratios of 1/1, 1/2, 1/4 and 1/8 are available by programming DB1 and DB0 at I/O address 145. The microprocessor, U1, supplies the input clock at 6.144 MHz but the internal frequency range for U23 is 0.4 to 1.1 MHz. A divide ratio of 1/8 should be chosen. The proper bit pattern is DB1 = 1 and DB0 = 1 at I/0 address 145.

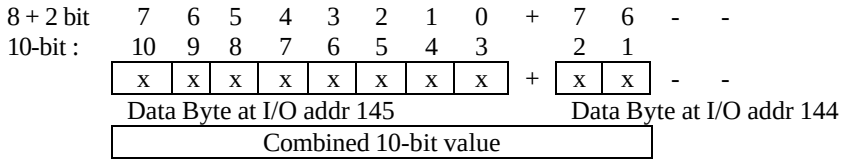
RATIO	**DB1**	**DB0**	**FREQ (MHz)**	
1/1	0	0	6.144	
1/2	0	1	3.072	
1/4	1	0	1.536	
1/8	1	1	0.768	Use **OUT 145,3**

The A/D Converter provides 8 data channels designated 0 through 7. The channels are program selectable by writing to data bits DB0 (1sb), DB1 and DB2 (msb) at I/O address 144. A single BASIC command can be used. For example, to select channel 4, the BASIC command would be **OUT 144,4.**

INITIALIZE BEFORE READING: Each reading must be preceded by an initialization sequence that sets the data format, divide ratio and selects the channel number. A typical sequence would be:

OUT 145,3 for binary data & divide ratio of 1/8, followed by
OUT 144,X where X is the channel number, o-7

ACQUIRE DATA: The incoming analog data on a channel is converted to 10-bits of digital data when the data registers are read at I/O addresses 145 and 144. The more significant 8 bits (10 to 3) are placed in the data byte at I/O address 145 and the two less significant bits (2 and 1) are carried in DB7 and DB6 of I/O address 144. The following diagram provides a graphic representation.



The software to acquire the two data bytes is trivial, but combining the bytes into a coherent 10-bit value may require some explanation. Assuming that variable Q1 and Q2 are used to acquire the data at addresses 145 and 144, then:

Q1 = INP (145) :Q1 will contain bits 3-10
Q2 = INP (144) :Q2 will contain bits 2-1 (bit positions 7 & 6)

CONVERT TO 10-BITS: To create the corresponding 10-bit data word, the data byte at I/O 145 needs to be pushed (rotated) 2 positions left. This can be accomplished in decimal format by multiplying "A" by 4 -- the decimal value corresponding to the 2 binary positions that are offset. Similarly, the data byte an I/O 144 must be pushed (rotated) right from positions 7 and 6 to 1 and 0. To make the adjustment, "B" should be divided by 64, the decimal equivalent of a 6-position binary offset. The 10-bit result can be expressed by variable C, in counts, as:

Q3 = (A*4) + (B/64)

Convert to Voltage: The voltage, V, can be calculated by dividing the count value by the total number of bits, 1024, and multiplying by the reference voltage:

V = Q3 * Vref / 1024

SOFTWARE: The A/D converter can be initialized and read with OUT and INP commands. The program shown below reads the voltage on a selected channel ten times. It calculates and displays the average value along with the maximum and minimum readings. Here are some comments about the logic used in the program:

Line 10: Variable Q contains the inputted channel number (0-7).

Line 20: The **OUT** statements initialize the converter:
At I/O address 145: DB2=0: Binary data format
At I/O address 145: DB2 and 1=1: Divide Ratio 1/8
At I/O address 144: Q: Channel Number

Line 23: The high & low data bytes are **INPut** to I/O addresses 145 and 144 as counts. Q1 = data bits 3-10. Q2 = data bits 2 and 1, but in bit positions 7 and 6.

Line 30: The data bytes are reconciled to a 10-bit number (Q3) as described on pages 2 and 3. The 10-bit count value is multiplied by 4.00/1024, the calibration factor for a reference voltage of 4.00 and 10-bits of resolution.

Lines 35-38: The minimum & maximum readings are determined for each iteration of the loop and stored in Q0 (min) and Q9 (max).

Lines 39-42: The sum of the readings is accumulated in Q4 - and then divided by the number of readings to calculate and print the average reading.

Lines 44-50: The maximum and minimum readings are displayed along with the maximum-to-minimum difference.

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TEST PROGRAM - A/D CONVERTER

```
10  PRI "A/D CONVERTER: ENTER CHANNEL #(0-7): ";:INPUT Q
12  QO=0:Q1=0:Q2=0:Q3=0:Q4=0:Q9=0
15  FOR 1=1 TO 10
20  OUT 145,3:OUT 144,Q
23  Q1=1NP(145):Q2=INP(144)
30  Q3=(Q1*4+Q2/64)*4.00/1024: 'Assumes Vref = 4.0v
34  PRI Q3
35  IF 1=1 THEN Q0=Q3
36  IF 1=1 THEN Q9=Q3
37  IF Q3 <Q0 THEN Q0=Q3
38  IF Q3 > Q9 THEN Q9=Q3
39  Q4=Q4+Q3
40  NEXT 1
42  PRI:PRI "AVG: ";Q4/10
44  PRI:PRI "MAX: ";Q9
46  PRI "MIN: ";Q0
48  PRI "DIFF: ";Q9-Q0
50  PRI "%DIF: ";(Q9-Q0)*100*1/(Q4*2);"%"
52  PRI:PRI:GOTO 10
```

CALIBRATION: The A/D converter should be calibrated with a known voltage source. It is possible to use a common 1.5 volt flashlight battery such as a AA, C or D cell. Typically, a fresh zinc-carbon battery reads 1.55 volts. Connect the '+' side of the battery to an input pin in the inner row of J1 and negative side to a pin in the outer row. Channel 4 affords a convenient connection.

Using a high impedance DC voltmeter, set the reference voltage at U23, pin 5, to 4.0 volts DC by adjusting trimpot POT2. Minimum (data sheet) setting is 4.0; maximum at 5.0. The reference voltage will determine the highest voltage that can be measured.

Type the program above into RAM memory. **RUN** the program while observing the displayed **AVG** reading. Re-adjust POT2 slightly until 3 or 4 **RUNs** produce an **AVG** reading that centers at 1.55 volts. To lower the displayed reading, turn the POT2 adjustment screw clockwise; to raise, counter-clockwise. This completes an absolute calibration assuming that the battery's output is 1.55 volts DC.

It may be more useful to calibrate the system relative to a meter that will measure the analog signals to be digitized. For relative calibration, use the reference meter to measure the battery voltage. When **RUNning** the program, adjust POT1 until the **AVG** reading centers on the measured reading instead of the assumed 1.55 volts.

CONNECTIONS TO DATA INPUT: Two common methods of connection are ribbon cable and twisted wire pairs. For ribbon cable, install the 2 x 10 pin header. An IDC connector can be used to attach the ribbon cable to the header strip. Note that every other lead will be connected to ground via the pins in row 1. The opposite ends of the grounded leads should be connected to the ground of the analog circuitry. For twisted pairs, delete the header and install the positive lead of the twisted pair in the appropriate hole in row 2 and the ground lead in row 1. It is good practice to ground all unused channels to avoid crosstalk. Shorting blocks can be used at connector J12.

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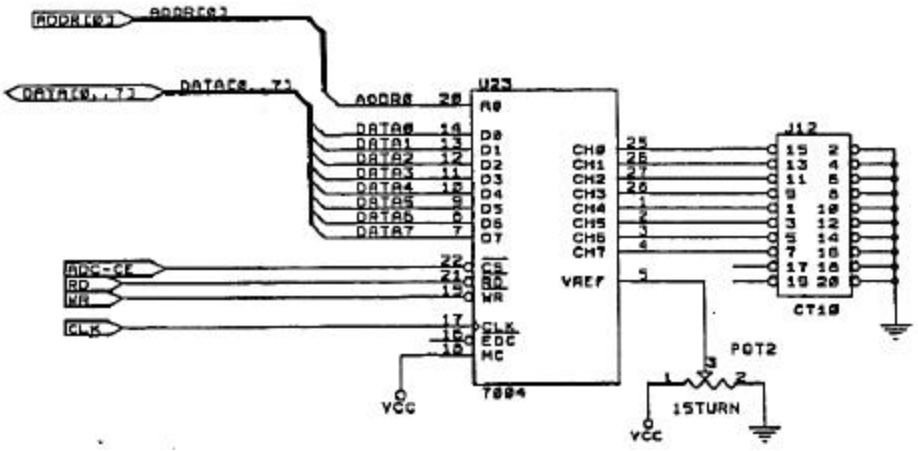
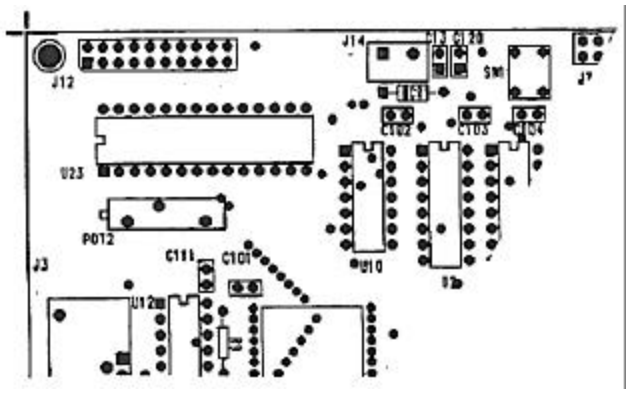
MEASUREMENT: Each of the eight channels is capable of measuring an analog voltage between 0 and the reference voltage. The reference voltage limits are +4.0 to +5.0 vdc (VDD).

SCHEMATIC DIAGRAM



COMPONENT ARRANGEMENT DIAGRAM



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μPD7004
10-BIT CMOS SUCCESSIVE APPROXIMATION A/D CONVERTER

NEC Electronics Inc.

September 1985

Description

The μPD7004 is a 10-bit monolithic CMOS analog-to-digital converter using the Successive Approximation Register (SAR) technique. The μPD7004 incorporates an 8-channel multiplexed analog input and full microprocessor interface to achieve a high degree of versatility. The designer has a choice of either serial or parallel output and interface to 8080 type microprocessors or advanced signal processors like the μPD7720.

Features

- ☐ 8-channel multiplexed analog input
- ☐ Serial or parallel interface
- ☐ 10-bit resolution
- ☐ Linearity: 1 LSB max. (T_A = 25°C)
- ☐ Conversion time: 100 μs (f_{CLK} = 1 MHz)
- ☐ Input voltage range 0 to V_{DD}
- ☐ Temperature range from -40 to +85°C
- ☐ Operates from single +5 volt supply

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7004C	Plastic DIP	-40°C to +85°C

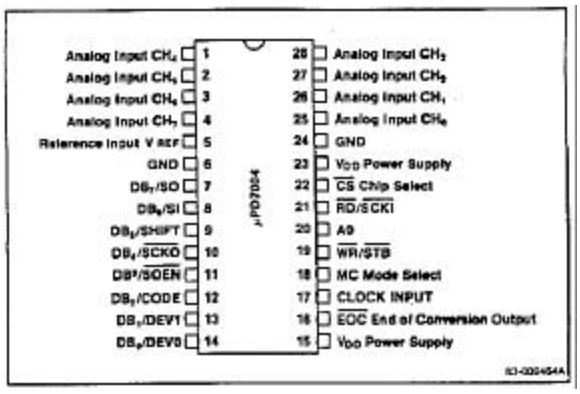
Absolute Maximum Ratings

T_A = 25°C

Supply Voltage, V_{DD}	-0.3 to +7.0 V
Input Voltage V_I	-0.3 to V_{DD} + 0.3 V
Reference Voltage, V_{REF}	-0.3 to V_{DD} + 0.3 V
Operating Temperature, T_{OPT}	-40 to + 85°C
Storage Temperature, T_{OPT}	-65 to +125°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Conversion Characteristics

T_A = 25°C, V_{DD} = V_{REF} = 4.5 to 5.5 V, f_{CKI} = 1 MHz

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution		10	10	10	Bit	-40~+85°C
Nonlinearity	HL	-1.0		1.0	LSB	
Zero Scale Error		-0.5		0.5	LSB	
Zero Scale Temperature Coefficient			2		ppm /°C	-40~+85°C
Full Scale Error		-0.5		0.5	LSB	
Full Scale Temperature Coefficient	$\frac{\Delta I_{FS}}{I_{FS}\cdot\Delta T}$		2		ppm /°C	-40~+85°C
Nonlinearity		-2		2	LSB	-40~+85°C (T=T_{OPT})

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μPD7004

Pin Identification

		Parallel Mode		Serial Mode	
Pin	Symbol	Direction	Function	Direction	Function
1	CH4		Analog input CH4		
2	CH5		Analog input CH5		
3	CH6		Analog input CH6		
4	CH7		Analog input CH7		
5	$V+_{REF}$		Positive reference input		
6	GND		Ground		
7	DB7/SO	O	Data bus (MSB)	O	Serial output
8	DB6/SI	O	Data bus (2nd)	I	Serial input
9	DB5/SHIFT	O	Data bus (3rd)	I	LSB/MSB 1st select
10	DB4/SCKO	O	Data bus (4th)	I/O	Serial clock output
11	DB3/SOEN	O	Data bus (5th)	I/O	Serial output enable
12	DB2/CODE	I/O	Data bus (6th)	I	Code select
13	DB1/DEVI	I/O	Data bus (7th	I	Frequency divide ratio set
14	DBO/DEVO	I/O	Data bus (LSB)	I	Frequency divide ratio set
15	VDD		Power supply		
16	EOC	O	End of conversion (active low)		
17	CLOCK	I	Clock input		
18	MC	I	MODE select (H=Parallel, L=Serial)		
19	WR/STB	I	Write input	I	Strobe input
20	AO	I	Address input	I	Internal/external shift clock
21	RD/SCKI	I	Read input	I	Serial clock input
22	CS	I	Chip select		
23	VDD		Power supply		
24	GND		Ground		
25	CHO		Analog input CH0		
26	CH1		Analog input CH1		
27	CH2		Analog input CH2		
28	CH3		Analog input CH3		

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µPD7004

DC Characteristics

T_A = -40°C to +85°C, V_{PEF} = 5.0 ± 0.5 V, f_{ds} = 1 MHz

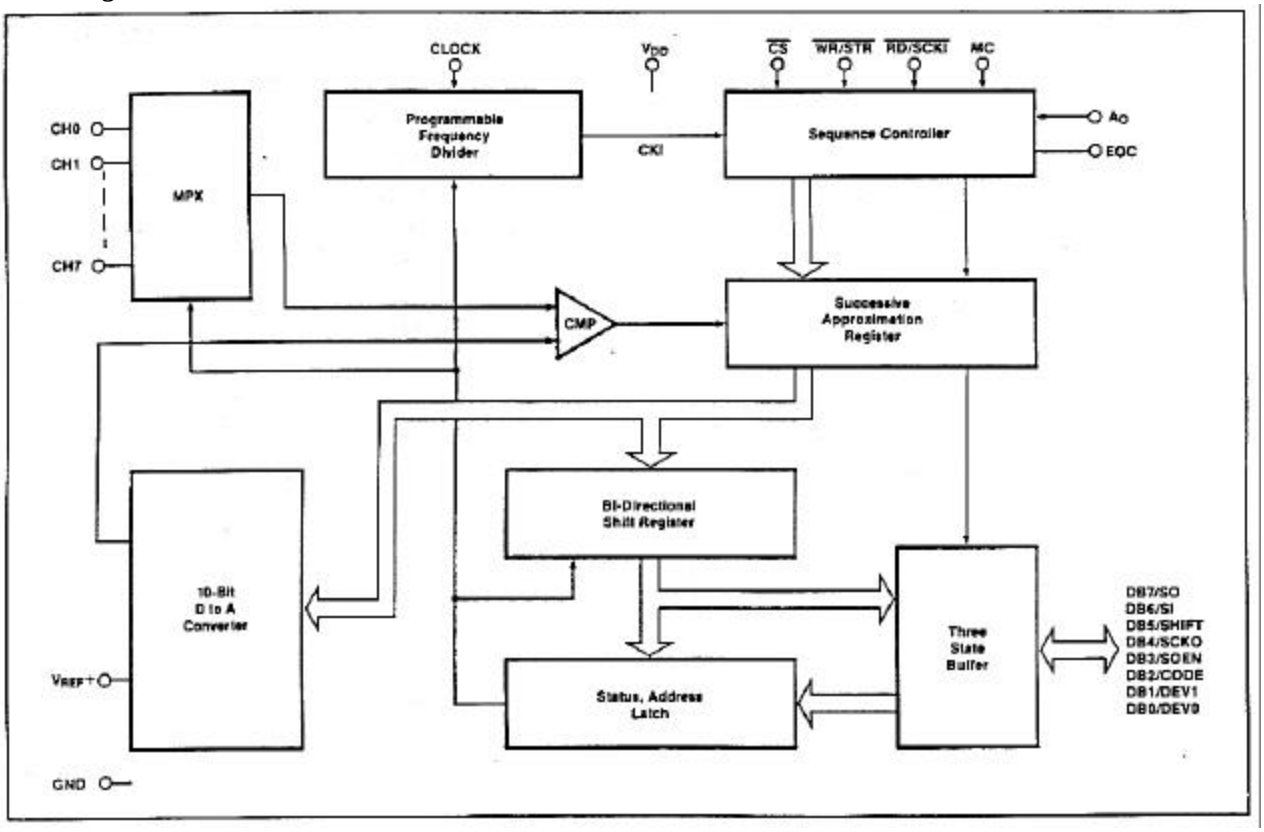
Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
High Level Output Voltage	V_{OH}	3.5			V	I_O = -1.6 mA
Low Level Output Voltage	V_{OL}			0.4	V	I_O = 1.6 mA
Digital Input Leakage Current	I_{ID}	-10		10	µA	V_I = O V_{DD}
High-Z Output Leakage Current	I_{FO}	-10		10	µA	V_O = O V_{DD}
Analog Input Resistance	RI(DC)		1000		MΩ	V_I = O V_{DD}
Equivalent Analog Input Resistance	R_I		10		kΩ	Analog input impedance is equivalent to that of the series circuit of R_I and C_I
	C_I		100		pF	
Reference Input Resistance	R_{REF}	5		50	kΩ	
Power Dissipation	P_O		5	15	mW	

Recommended Operating Conditions

T_A = -20°C to +80°C

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Reference Voltage	V_{REF}	4.0		V_{DD}	V	
Analog Input Voltage	V_I	0.0		V_{REF}	V	
High Level Input Voltage	V_{IH}	2.4			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Clock Frequency	f_{CK}	0.4		8.8	MHz	
Internal Clock Frequency	f_{ICK}	0.4	1.0	1.1	MHz	f_{ICK} = f_{CK} X Divide Ratio
Parallel Mode (MC = High)						
Address Setup Time	t_{AW}	50			n$	CS ↑. AO → WR ↓
	t_{AR}	50			n$	CS ↑. AO → RD ↓
Address Hold Time	t_{WA}	50			n$	WR ↑ → CS ↓ AO
	t_{RA}	50			n$	RD ↑ → CS ↓ AO
WR Pulse Width	t_{WW}	400			n$	
RD Pulse Width	t_{BR}	400			n$	
Data Setup Time	t_{DW}	300			n$	DB → WR ↑
Data Hold Time	t_{WD}	100			n$	WR ↑ → DB

Block Diagram



AC Characteristics

T_A = -40°C to +85°C, V_{DD} = V_{REF} = 5 ± 0.5 V1 f_{ckI} = 1 MHz

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Delay Time	tRD			250	n$	RD DB (parallel mode)
	tDKO			250	n$	SCKI , SCKO SO (serial mode)
Output Floating Delay Time	tDF			150	n$	RD OB floating (parallel mode)
	tFCSO			150	n$	CS SO floating (serial mode 1)
Serial Clock Output Delay Time	tSKS	40		200	n$	SCKO SOEN (serial mode 2)
Serial Output Enable Delay Time	tHKS	0		200	n$	SCKO SPEM (serial mode 2)
Serial Clock Output Cycle	tCYK		1/fCKI		n$	(Serial mode 2)
High Level Serial Clock Pulse Width	tWHK	400			n$	(Serial mode 2)
Low Level Serial Clock Pulse Width	tWLK	400			n$	(Serial mode 2)
Serial Clock Rise Time	tRSC		20		n$	(Serial mode 2)
Serial Clock Fall Time	tFSC		20		n$	(Serial mode 2)

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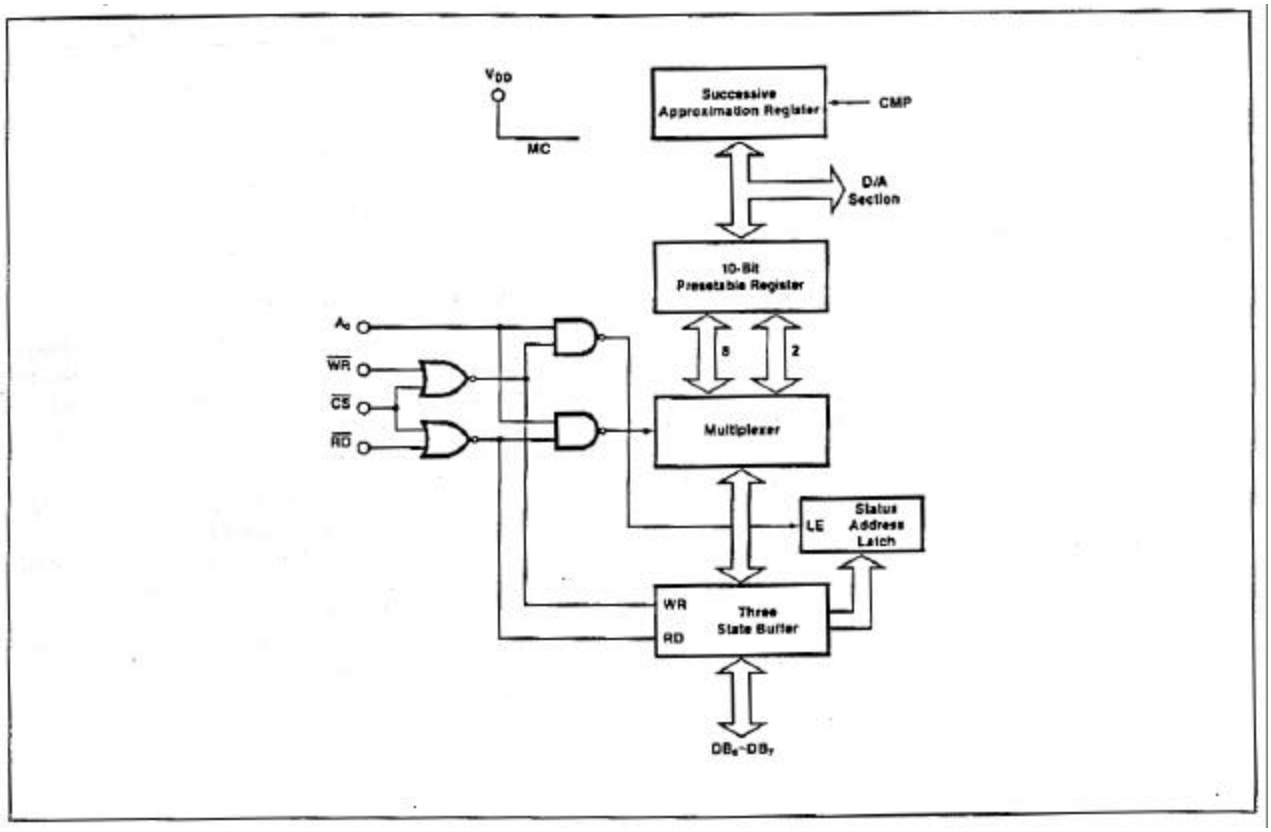
uPD7004

Data Bus I/O Operation (Parallel Mode MC = H)

Pin	Symbol				Function			
22	CS	H	L	L	L	L	L	L
19	WR	x	H	L	L	H	H	L
21	RD	x	H	H	H	L	L	L
20	AO	x	x	H	L	H	L	X
--	Operation		No Operation	Initialize	MPX address setting	High byte road	Low byte road	Inhibit
7	DB7	--	--	DB2 = CODE select	DB2.1.0 = Analog	DB7 - DB0	DB7.DB6	
:	:	:	:	H = 2's comp	CH select	= MSB - 8th	=9th, LSB	
:	:	:	:	L = binary	0, 0, 0 - 1, 1, 1		DB5 - DB0	
:	:	:	:	DB1, DB0 = divide ratio	= CH0 - CH7		= LOW level	
:	:	:	:	0, 0 - 1, 1				
14	DB0	--	--	=1/1 - 1/8				

Parallel Operation



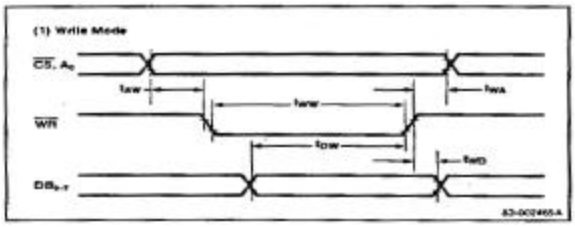
Addressing the Inputs

One of eight analog inputs can be selected with the µPD7004 in the "write" mode and A0 at pin 20 set "low." The "write" mode is selected by setting the Chip Select (CS) at pin 22, and Write (WR) at pin 19, "low" or 0. The multiplex channel select is accomplished by presenting a 3-bit binary code to DB0 to DB2 at pins 14, 13, and 12 where 000 = channel 0 and 111 = channel 7.

Referring to figure 1, the sequence is:

- ☐ Chip Select (CS) and A0 set "low."
- ☐ Write (WR) set "low." (Read (RD) is left "high.")
- ☐ Analog input channel selected by presenting a 3-bit binary code on pins 14, 13, 12 (D0 to D2).
- ☐ The address is latched and the desired input channel is now selected.

Figure 1. Write Mode Timing Diagram



Initializing the Converter

The µPD7004 gives the designer a choice of the type of data output format, either a 2's complement or binary, and the speed of operation by providing a programmable frequency divider. These options may be selected by the controlling system at any time by the "initialize" mode.

The "initialize mode" is set with CS and WR both "low." RD and A0 are set "high." Code select is accomplished by presenting either a "high" for 2's complement or "low" for binary output at DB2 (pin 12). The divide ratio of 1/1 to 1/8 is set by presenting a 2-bit code to DB0 (pin 14) and DB1 (pin 13).

Ratio	DB0	DB1
1/1	L	L
1/2	H	L
1/4	L	H
1/8	H	H

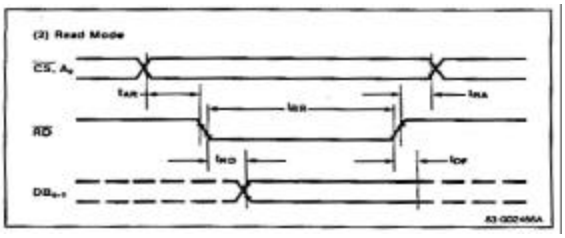
Data Output

Data can be read in 2 bytes from the data output at pins 7 through 14 (DB7 to DB0). To read the high byte, CS and RD are both "low." To read the low byte, A0 is set Low and data bit 9 and 10 are present at DB7 and DB6 respectively. During the low data byte read DB0 through DB5 are "low".

Referring to figure 2, the sequence is:

- ☐ Chip Select (CS) "low" and A0 (pin 20) "high"
- ☐ Read (RD) set "low" and Write (WR) set "high"
- ☐ Output high byte (MSB to 8th bit)
- ☐ A0 set "low"
- ☐ Output low byte (9th bit and LSB)

Figure 2. Data Output Timing Diagram



The Conversion Sequence

The µPD7004C uses the Successive Approximation Register (SAR) technique to convert analog voltage levels to 10-bit digital code in either 2's complement or binary format. Regardless of the type of data output (either serial or parallel), the conversion process is the same.

Once the clock frequency and the output data format have been set, and the analog input selected, the conversion process begins with the analog level compared to the existing level from an internal 10-bit digital to analog converter. The D/A output level is proportional to the existing code output from the Successive Approximation Register which is proportional to the input level from the comparator.

Timing Waveforms (Cont.)

Parallel Mode Timing Chart (MC = H)